

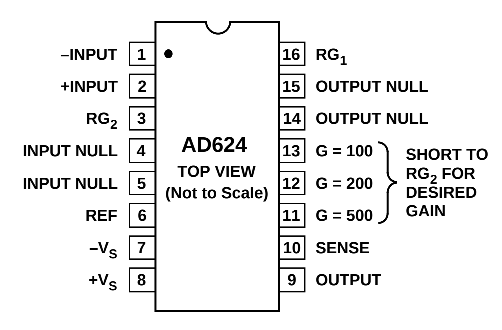
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2 μV p-p 0.1 Hz to 10 Hz
Low Gain TC: 5 ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130 dB min (G = 500 to 1000)
Low Input Offset Voltage: 25 μV, max
Low Input Offset Voltage Drift: 0.25 μV/°C max
Gain Bandwidth Product: 25 MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The AD624 is a high precision, low noise, instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25 μV/°C, output offset voltage drift of less than 10 μV/°C, CMRR above 80 dB at unity gain (130 dB at G = 500) and a maximum nonlinearity of 0.001% at G = 1. In addition to these outstanding dc specifications, the AD624 exhibits superior ac performance as well. A 25 MHz gain bandwidth product, 5 V/μs slew rate and 15 μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pretrimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than 4 nV/$\sqrt{Hz}$ at 1 kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pretrimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

REV. B

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AD624–SPECIFICATIONS (@ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C, unless otherwise noted)

Model	AD624A Min	Typ	Max	AD624B Min	Typ	Max	AD624C Min	Typ	Max	AD624S Min	Typ	Max	Units
GAIN													
Gain Equation													
(External Resistor Gain Programming)	$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			
Gain Range (Pin Programmable)	1 to 1000			1 to 1000			1 to 1000			1 to 1000			
Gain Error													
G = 1			**±0.05**			**±0.03**			**±0.02**			**±0.05**	%
G = 100			**±0.25**			**±0.15**			**±0.1**			**±0.25**	%
G = 200, 500			**±0.5**			**±0.35**			**±0.25**			**±0.5**	%
Nonlinearity													
G = 1			±0.005			±0.003			±0.001			±0.005	%
G = 100, 200			±0.005			±0.003			±0.001			±0.005	%
G = 500			±0.005			±0.005			±0.005			±0.005	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 100, 200			10			10			10			10	ppm/°C
G = 500			25			15			15			15	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			**200**			**75**			**25**			**75**	µV
vs. Temperature			**2**			**0.5**			**0.25**			**2.0**	µV/°C
Output Offset Voltage			**5**			**3**			**2**			**3**	mV
vs. Temperature			**50**			**25**			**10**			**50**	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	**70**			**75**			**80**			**75**			dB
G = 100, 200	**95**			**105**			**110**			**105**			dB
G = 500	**100**			**110**			**115**			**110**			dB
INPUT CURRENT													
Input Bias Current			**±50**			**±25**			**±15**			**±50**	nA
vs. Temperature		±50			±50			±50			±50		pA/°C
Input Offset Current			**±35**			**±15**			**±10**			**±35**	nA
vs. Temperature		±20			±20			±20			±20		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common-Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common-Mode Capacitance		10			10			10			10		pF
Input Voltage Range[1]													
Max Differ. Input Linear (V_{DL})	±10			±10			±10			±10			V
Max Common-Mode Linear (V_{CM})		$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$		V
Common-Mode Rejection dc to 60 Hz with 1 kΩ Source Imbalance													
G = 1	**70**			**75**			**80**			**70**			dB
G = 100, 200	**100**			**105**			**110**			**100**			dB
G = 500	**110**			**120**			**130**			**110**			dB
OUTPUT RATING													
V_{OUT}, R_L = 2 kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal –3 dB													
G = 1		1			1			1			1		MHz
G = 100		150			150			150			150		kHz
G = 200		100			100			100			100		kHz
G = 500		50			50			50			50		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step													
G = 1 to 200		15			15			15			15		µs
G = 500		35			35			35			35		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1 kHz													
R.T.I.		4			4			4			4		nV/$\sqrt{Hz}$
R.T.O.		75			75			75			75		nV/$\sqrt{Hz}$
R.T.I., 0.1 Hz to 10 Hz													
G = 1		10			10			10			10		µV p-p
G = 100		0.3			0.3			0.3			0.3		µV p-p
G = 200, 500, 1000		0.2			0.2			0.2			0.2		µV p-p
Current Noise													
0.1 Hz to 10 Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12	kΩ
I_{IN}		30			30			30			30		µA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%

Model	AD624A			AD624B			AD624C			AD624S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
REFERENCE INPUT													
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24	kΩ
I_{IN}		30			30			30			30		µA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	–25		+85	–25		+85	–25		+85	–55		+125	°C
Storage	–65		+150	–65		+150	–65		+150	–65		+150	°C
POWER SUPPLY													
Power Supply range	**±6**	**±15**	**±18**	**±6**	**±15**	**±18**	**±6**	**±15**	**±18**	**±6**	**±15**	**±18**	V
Quiescent Current		3.5	5		3.5	5		3.5	5		3.5	5	mA

NOTES

[1]V_{DL} is the maximum differential input voltage at G = 1 for specified nonlinearity, V_{DL} at other gains = 10 V/G. V_D = actual differential input voltage.
Example: G = 10, V_D = 0.50. V_{CM} = 12 V – (10/2 × 0.50 V) = 9.5 V.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production unit at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . ±18 V
Internal Power Dissipation . . . . 420 mW
Input Voltage . . . . $±V_S$
Differential Input Voltage . . . . $±V_S$
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range . . . . –65°C to +150°C
Operating Temperature Range
AD624A/B/C . . . . –25°C to +85°C
AD624S . . . . –55°C to +125°C
Lead Temperature (Soldering, 60 secs) . . . . +300°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

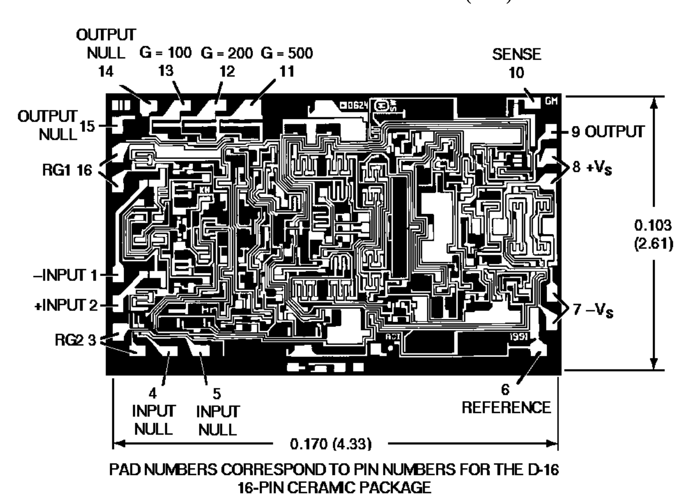
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD624AD	–25°C to +85°C	16-Pin Ceramic DIP	D-16
AD624BD	–25°C to +85°C	16-Pin Ceramic DIP	D-16
AD624CD	–25°C to +85°C	16-Pin Ceramic DIP	D-16
AD624SD	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD624SD/883B*	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD624SChips	–25°C to +85°C	Die	

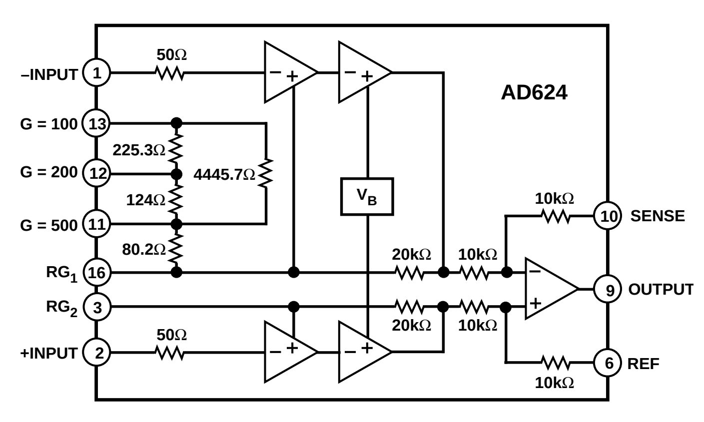
*See Analog Devices’ military data sheet for 883B specifications.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions
Dimensions shown in inches and (mm).

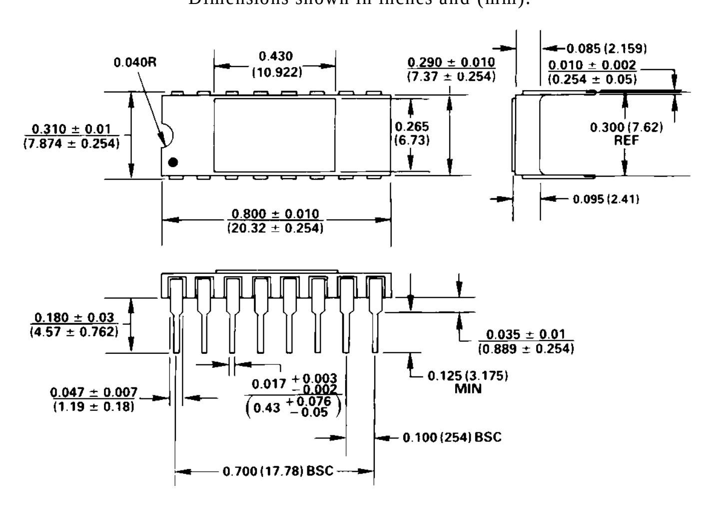


FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AD624–Typical Characteristics

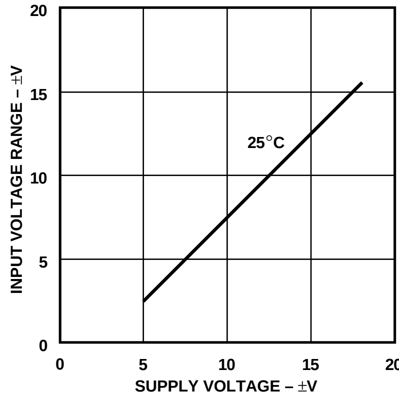


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

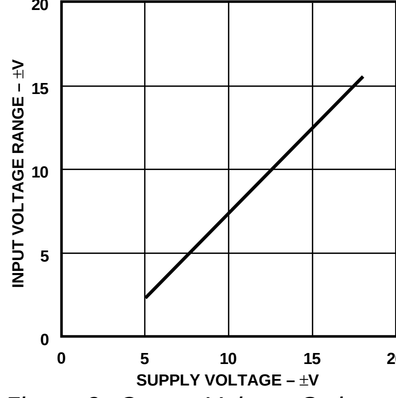


Figure 2. Output Voltage Swing vs. Supply Voltage

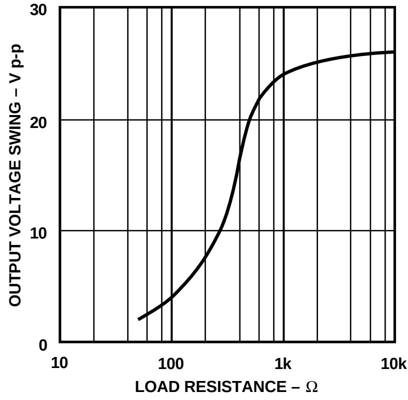


Figure 3. Output Voltage Swing vs. Load Resistance

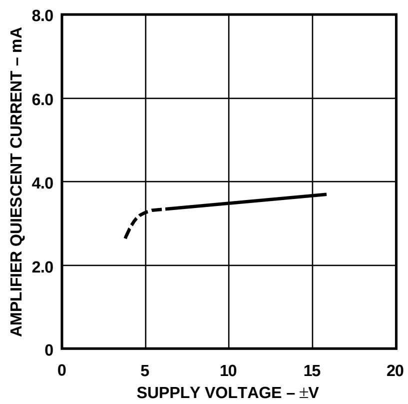


Figure 4. Quiescent Current vs. Supply Voltage

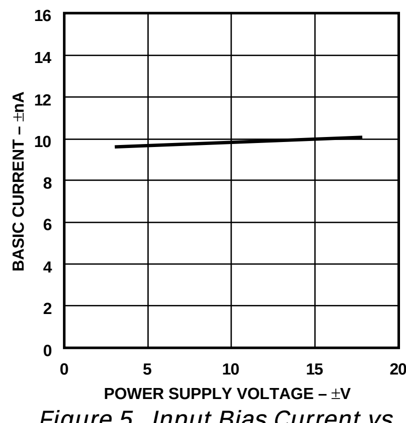


Figure 5. Input Bias Current vs. Supply Voltage

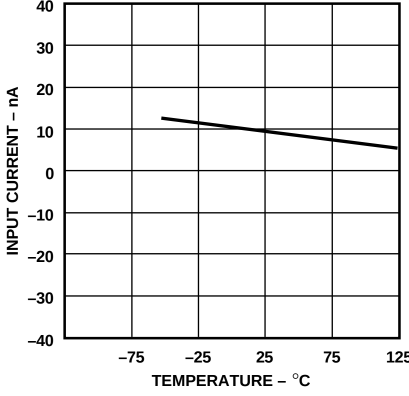


Figure 6. Input Bias Current vs. Temperature

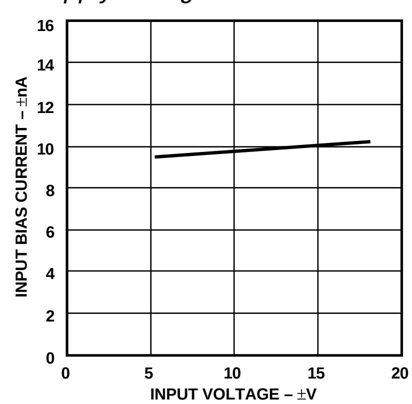


Figure 7. Input Bias Current vs. CMV

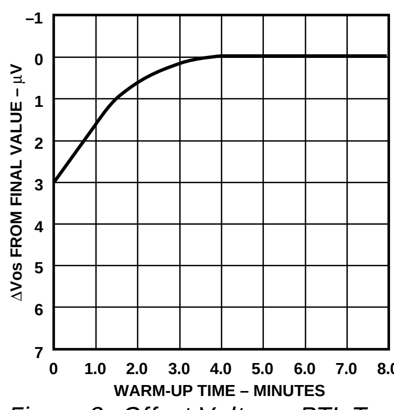


Figure 8. Offset Voltage, RTI, Turn On Drift

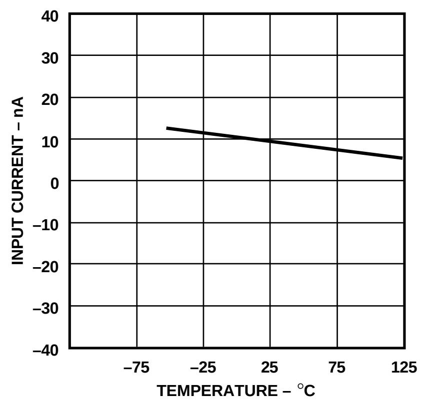


Figure 9. Gain vs. Frequency

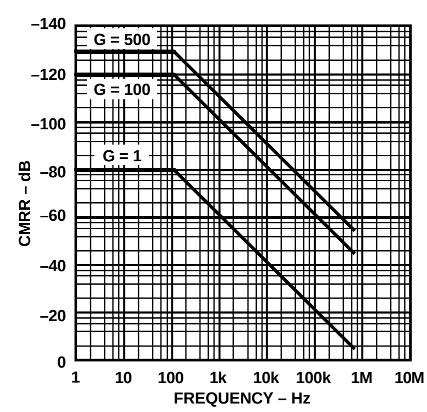


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

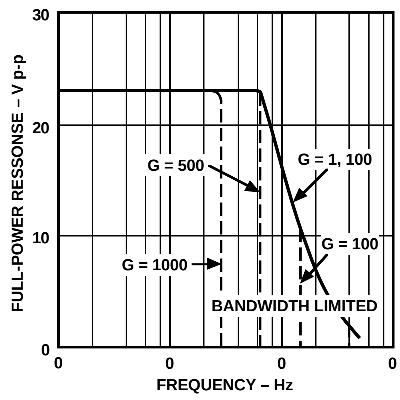


Figure 11. Large Signal Frequency Response

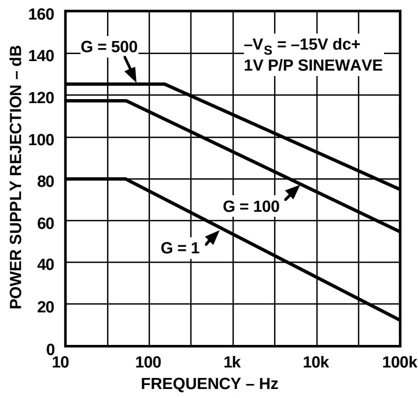


Figure 12. Positive PSRR vs. Frequency

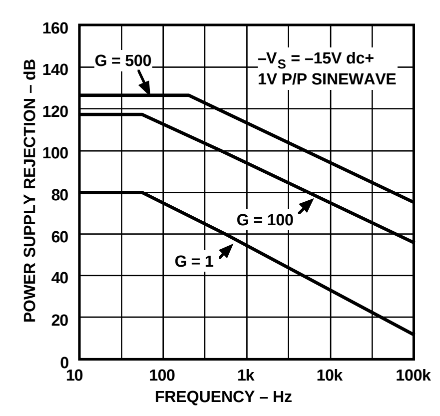


Figure 13. Negative PSRR vs. Frequency

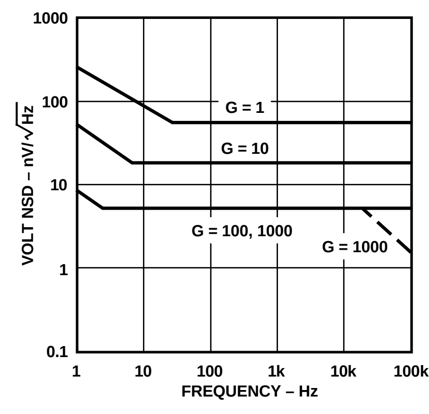


Figure 14. RTI Noise Spectral Density vs. Gain

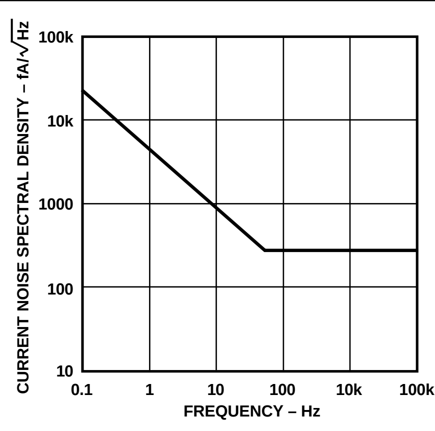


Figure 15. Input Current Noise

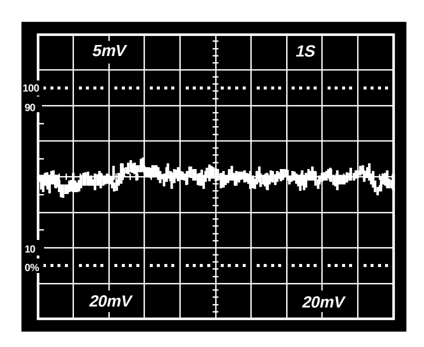


Figure 16. Low Frequency Voltage Noise, G = 1 (System Gain = 1000)

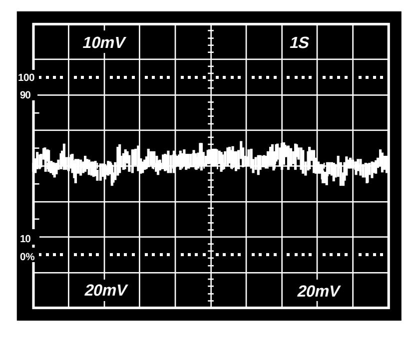


Figure 17. Low Frequency Voltage Noise, G = 1000 (System Gain = 100,000)

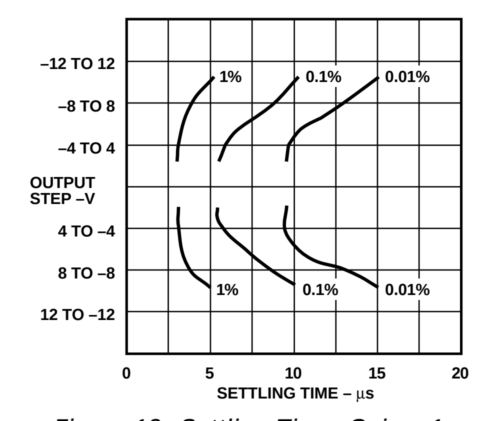


Figure 18. Settling Time, Gain = 1

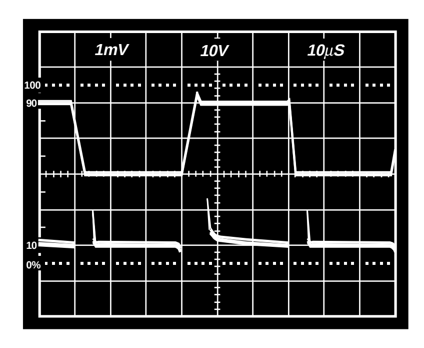


Figure 19. Large Signal Pulse Response and Settling Time, G = 1

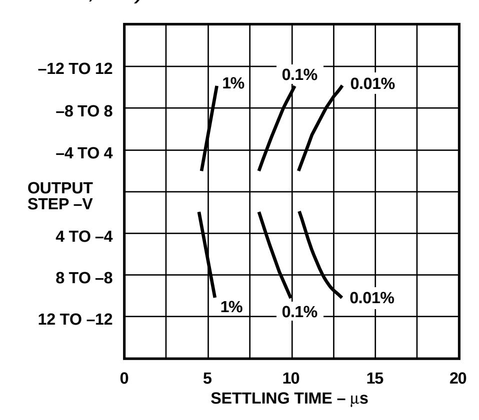


Figure 20. Settling Time Gain = 100

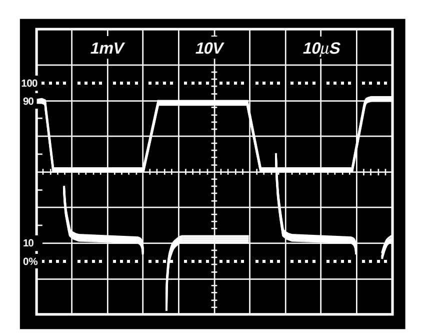


Figure 21. Large Signal Pulse Response and Settling Time, G = 100

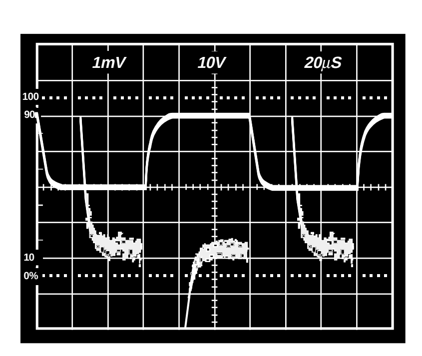


Figure 22. Range Signal Pulse Response and Settling Time, G = 500

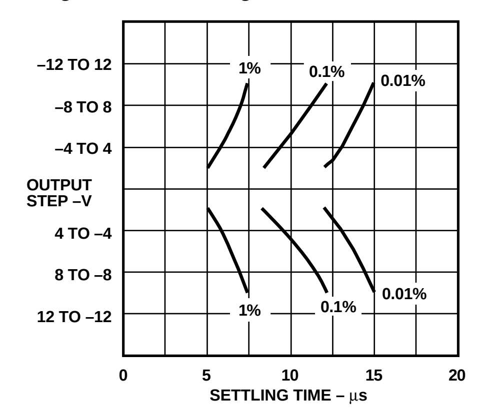


Figure 23. Settling Time Gain = 1000

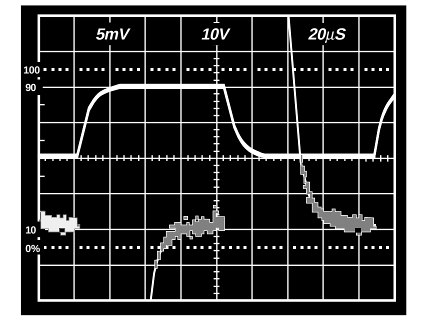


Figure 24. Large Signal Pulse Response and Settling Time, G = 1000

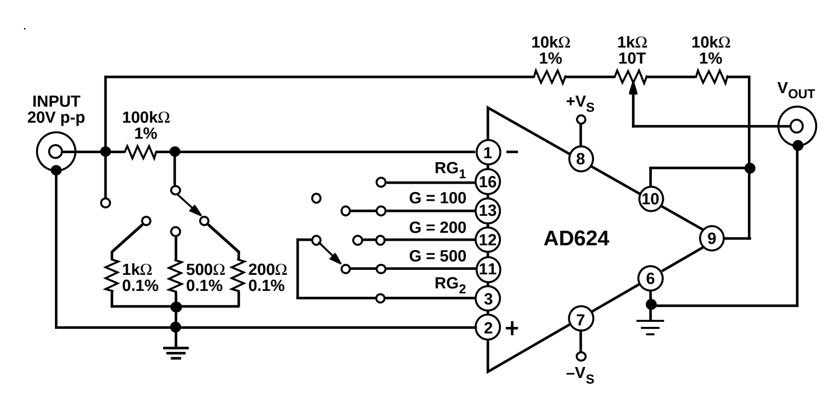


Figure 25. Settling Time Test Circuit

THEORY OF OPERATION

The AD624 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp instrumentation amplifier. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components and the high level of performance that this circuit architecture is capable of.

A preamp section (Q1–Q4) develops the programmed gain by the use of feedback concepts. Feedback from the outputs of A1 and A2 forces the collector currents of Q1–Q4 to be constant thereby impressing the input voltage across R_G.

The gain is set by choosing the value of R_G from the equation, Gain $= \frac{40\,k}{R_G} + 1$. The value of R_G also sets the transconductance of the input preamp stage increasing it asymptotically to the transconductance of the input transistors as R_G is reduced for larger gains. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 3 ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25 MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of 4 nV/$\sqrt{Hz}$ at G ≥ 500.

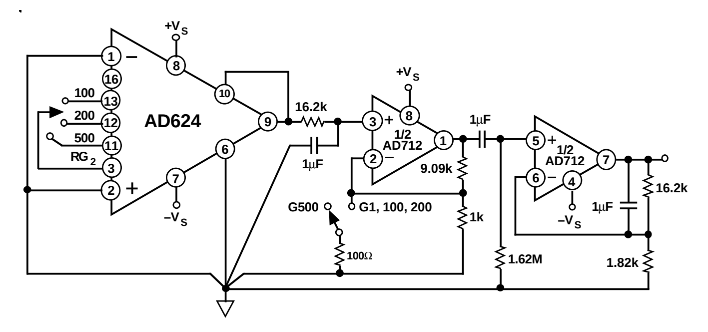


Figure 26. Noise Test Circuit

INPUT CONSIDERATIONS

Under input overload conditions the user will see R_G + 100 Ω and two diode drops (~1.2 V) between the plus and minus inputs, in either direction. If safe overload current under all conditions is assumed to be 10 mA, the maximum overload voltage is ~ ±2.5 V. While the AD624 can withstand this continuously, momentary overloads of ±10 V will not harm the device. On the other hand the inputs should never exceed the supply voltage.

The AD524 should be considered in applications that require protection from severe input overload. If this is not possible, external protection resistors can be put in series with the inputs of the AD624 to augment the internal (50 Ω) protection resistors. This will most seriously degrade the noise performance. For this reason the value of these resistors should be chosen to be as low as possible and still provide 10 mA of current limiting under maximum continuous overload conditions. In selecting the value of these resistors, the internal gain setting resistor and the 1.2 volt drop need to be considered. For example, to protect the device from a continuous differential overload of 20 V at a gain of 100, 1.9 kΩ of resistance is required. The internal gain resistor is 404 Ω; the internal protect resistor is 100 Ω. There is a 1.2 V drop across D1 or D2 and the base-emitter junction of either Q1 and Q3 or Q2 and Q4 as shown in Figure 27, 1400 Ω of external resistance would be required (700 Ω in series with each input). The RTI noise in this case would be

$$\sqrt{4\,KTR_{ext} + (4\,nV/\sqrt{Hz})^2} = 6.2\,nV/\sqrt{Hz}$$

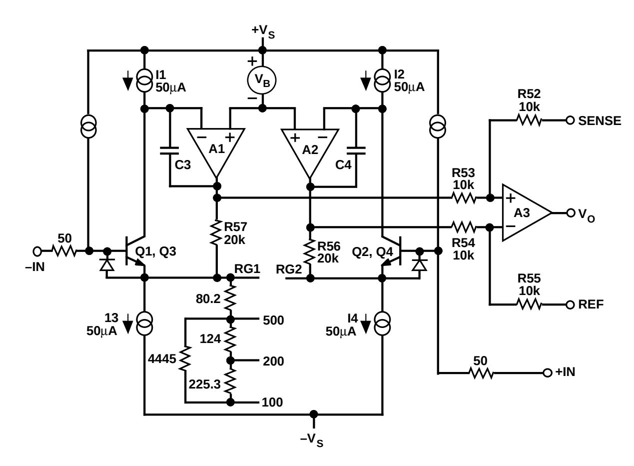


Figure 27. Simplified Circuit of Amplifier; Gain Is Defined as (R56 + R57)/(R_G) + 1. For a Gain of 1, R_G Is an Open Circuit.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift each have two components; input and output. Input offset is that component of offset that is

directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD624 might have a +250 µV output offset and a –50 µV input offset. In a unity gain configuration, the *total* output offset would be 200 µV or the sum of the two. At a gain of 100, the output offset would be –4.75 mV or: +250 µV + 100 (–50 µV) = –4.75 mV.

The AD624 provides for both input and output offset adjustment. This optimizes nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD624 includes high accuracy pretrimmed internal gain resistors. These allow for single connection programming of gains of 1, 100, 200 and 500. Additionally, a variety of gains including a pretrimmed gain of 1000 can be achieved through series and parallel combinations of the internal resistors. Table I shows the available gains and the appropriate pin connections and gain temperature coefficients.

The gain values achieved via the combination of internal resistors are extremely useful. The temperature coefficient of the gain is dependent primarily on the mismatch of the temperature coefficients of the various internal resistors. Tracking of these resistors is extremely tight resulting in the low gain TCs shown in Table I.

If the desired value of gain is not attainable using the internal resistors, a single external resistor can be used to achieve any gain between 1 and 10,000. This resistor connected between

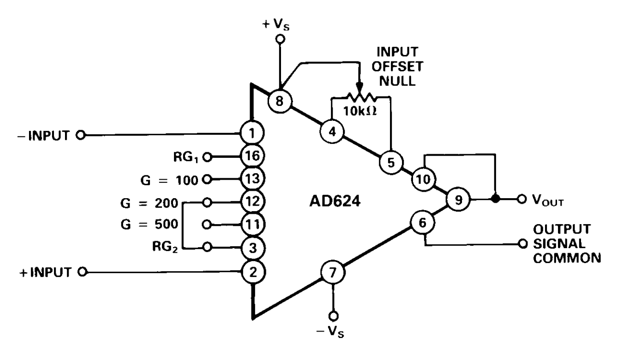


Figure 28. Operating Connections for G = 200

Table I.

Gain (Nominal)	Temperature Coefficient (Nominal)	Pin 3 to Pin	Connect Pins
1	–0 ppm/C	–	–
100	–1.5 ppm/°C	13	–
125	–5 ppm/°C	13	11 to 16
137	–5.5 ppm/°C	13	11 to 12
186.5	–6.5 ppm/°C	13	11 to 12 to 16
200	–3.5 ppm/°C	12	–
250	–5.5 ppm/°C	12	11 to 13
333	–15 ppm/°C	12	11 to 16
375	–0.5 ppm/°C	12	13 to 16
500	–10 ppm/°C	11	–
624	–5 ppm/°C	11	13 to 16
688	–1.5 ppm/°C	11	11 to 12; 13 to 16
831	+4 ppm/°C	11	16 to 12
1000	0 ppm/°C	11	16 to 12; 13 to 11

Pins 3 and 16 programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 29). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors R56 and R57. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (–15 ppm/°C typ), and the temperature coefficient of the internal interconnections .

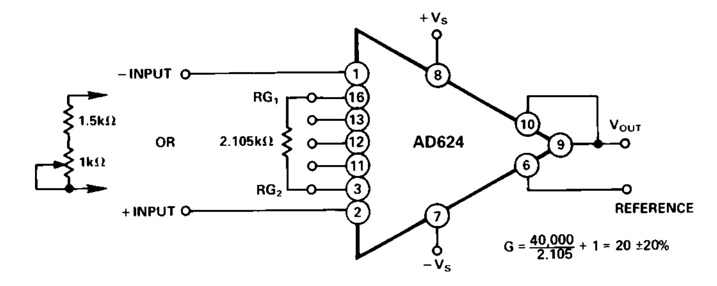


Figure 29. Operating Connections for G = 20

The AD624 may also be configured to provide gain in the output stage. Figure 30 shows an H pad attenuator connected to the reference and sense lines of the AD624. The values of R1, R2 and R3 should be selected to be as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

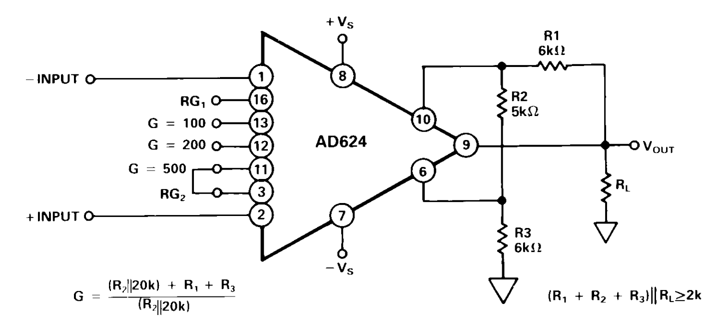


Figure 30. Gain of 2500

NOISE

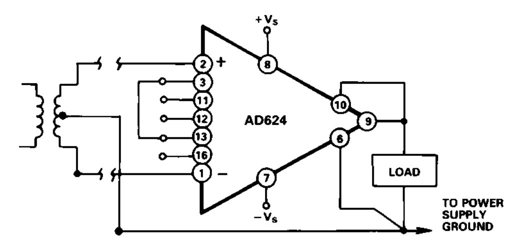
The AD624 is designed to provide noise performance near the theoretical noise floor. This is an extremely important design criteria as the front end noise of an instrumentation amplifier is the ultimate limitation on the resolution of the data acquisition system it is being used in. There are two sources of noise in an instrument amplifier, the input noise, predominantly generated by the differential input stage, and the output noise, generated by the output amplifier. Both of these components are present at the input (and output) of the instrumentation amplifier. At the input, the input noise will appear unaltered; the output noise will be attenuated by the closed loop gain (at the output, the output noise will be unaltered; the input noise will be amplified by the closed loop gain). Those two noise sources must be root sum squared to determine the total noise level expected at the input (or output).

The low frequency (0.1 Hz to 10 Hz) voltage noise due to the output stage is 10 μV p-p, the contribution of the input stage is 0.2 μV p-p. At a gain of 10, the RTI voltage noise would be 1 μV p-p, $\sqrt{\left(\frac{10}{G}\right)^2 + (0.2)^2}$. The RTO voltage noise would be 10.2 μV p-p, $\sqrt{10^2 + (0.2(G))^2}$. These calculations hold for applications using either internal or external gain resistors.

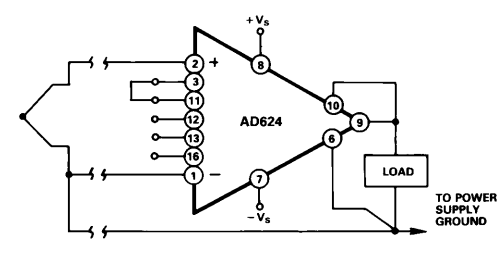
INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in a total error budget. The bias currents when multiplied by the source resistance imbalance appear as an additional offset voltage. (What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature.) Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source resistance.

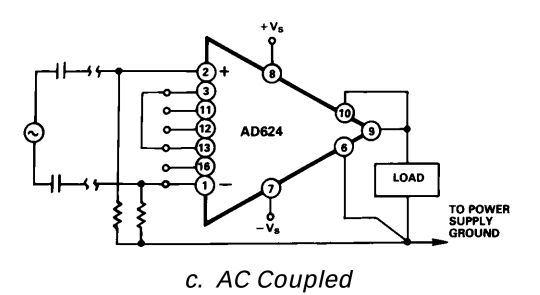
Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore,



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 31. Indirect Ground Returns for Bias Currents

when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground, (see Figure 31).

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80 dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

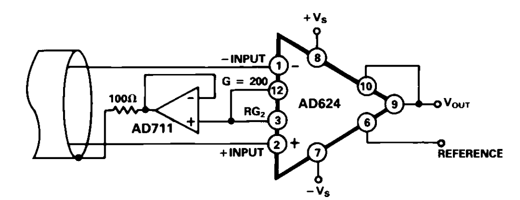


Figure 32. Shield Driver, G ≥ 100

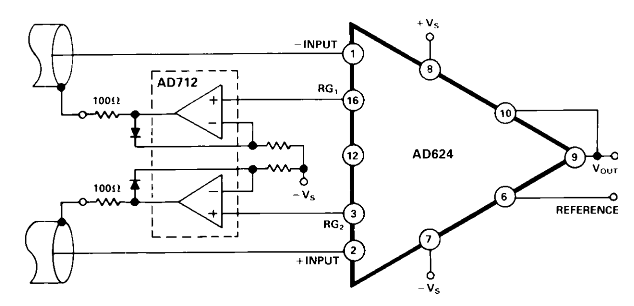


Figure 33. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths

have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the most sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors (see Figure 34).

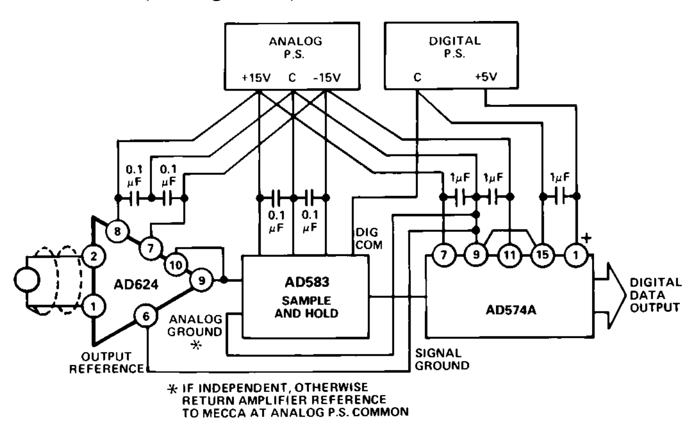


Figure 34. Basic Grounding Practice

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

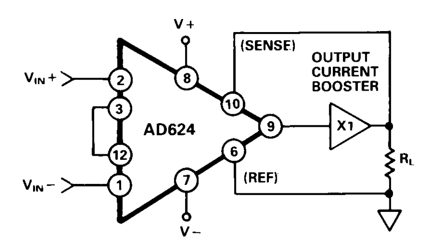


Figure 35. AD624 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2 kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 35 shows how a current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current without significantly degrading overall performance. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10 V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts, from ground, to be shared between signal and reference offset.

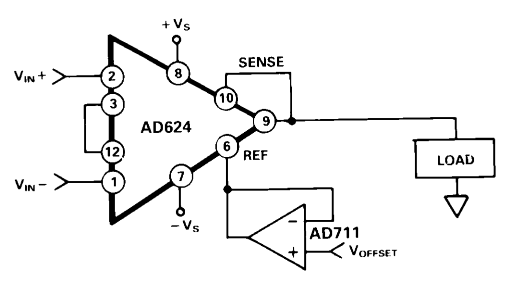


Figure 36. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance, including those caused by PC layouts or other connection techniques, which appears between the reference pin and ground will increase the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the IA. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD624 a reference source resistance will unbalance the CMR trim by the ratio of 10 kΩ/R_{REF}. For example, if the reference source impedance is 1 Ω, CMR will be reduced to 80 dB (10 kΩ/1 Ω = 80 dB). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 36. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 37.

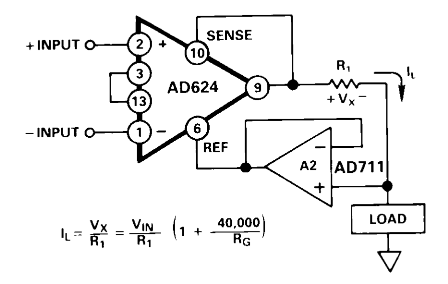


Figure 37. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 38 shows the AD624 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series

with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

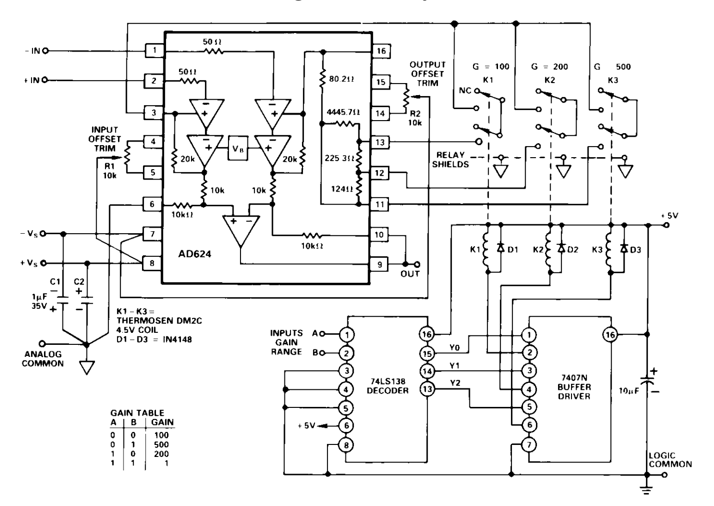


Figure 38. Gain Programmable Amplifier

A significant advantage in using the internal gain resistors in a programmable gain configuration is the minimization of thermocouple signals which are often present in multiplexed data acquisition systems.

If the full performance of the AD624 is to be achieved, the user must be extremely careful in designing and laying out his circuit to minimize the remaining thermocouple signals.

The AD624 can also be connected for gain in the output stage. Figure 39 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common-mode rejection ratio degradation.

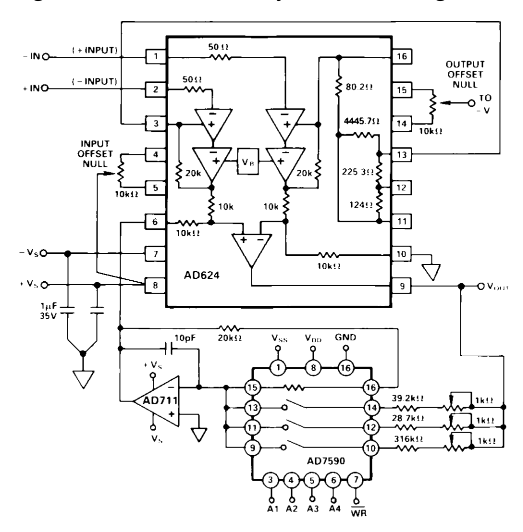


Figure 39. Programmable Output Gain

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

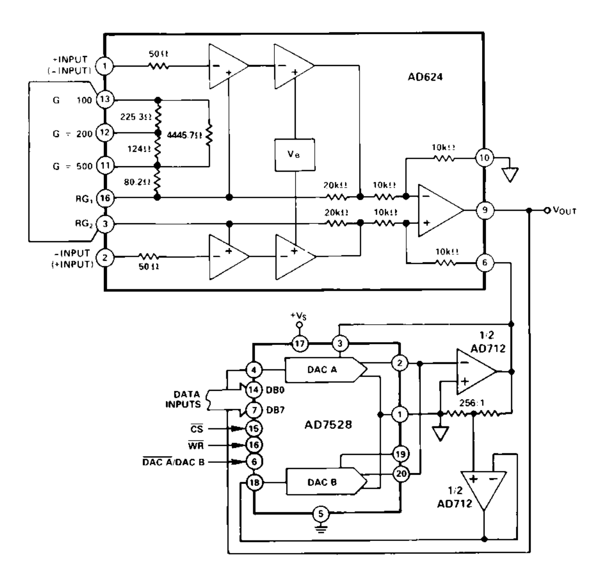


Figure 40. Programmable Output Gain Using a DAC

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 41 shows a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

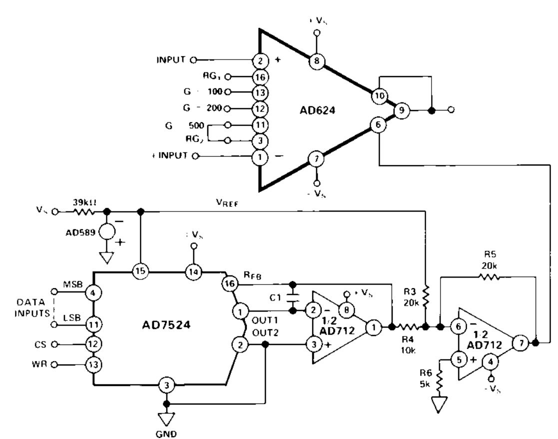


Figure 41. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For these applications Figure 42 provides a hardware solution.

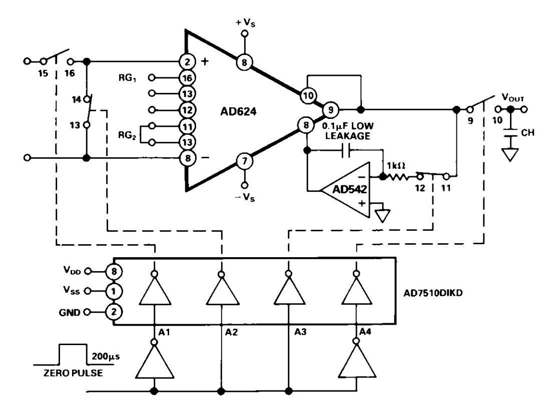


Figure 42. Auto-Zero Circuit

The microprocessor controlled data acquisition system shown in Figure 43 includes includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

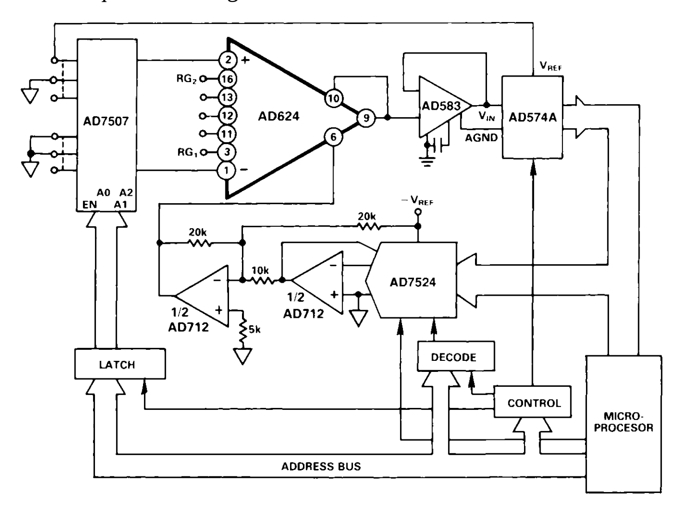


Figure 43. Microprocessor Controlled Data Acquisition System

WEIGH SCALE

Figure 44 shows an example of how an AD624 can be used to condition the differential output voltage from a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type particularly where it is desirable to measure small changes in weight as opposed to the absolute value. The addition of an auto gain/auto tare cycle will enable the system to remove offsets, gain errors, and drifts making possible true 14-bit performance.

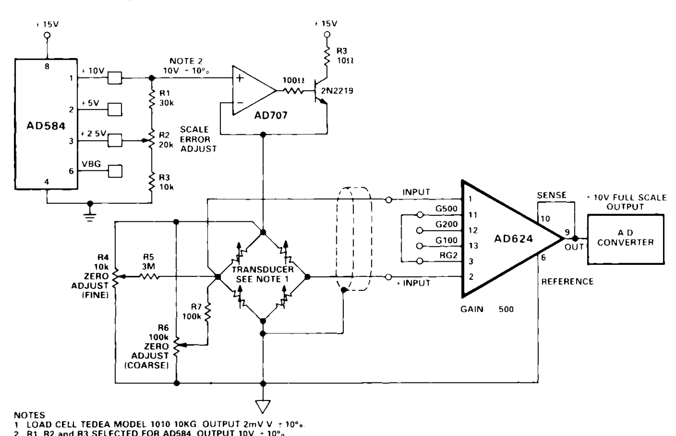


Figure 44. AD624 Weigh Scale Application

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, l/f noise, dc drifts in the electronics, and line noise pickup. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low-pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 45 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1 Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5 ppm change in bridge impedance. Such a change will produce a 6.3 mV change in the low-pass filtered dc output, well above the RTO drifts and noise.

The AC-CMRR of the AD624 decreases with the frequency of the input signal. This is due mainly to the package-pin capacitance associated with the AD624's internal gain resistors. If AC-CMRR is not sufficient for a given application, it can be trimmed by using a variable capacitor connected to the amplifier's RG_2 pin as shown in Figure 45.

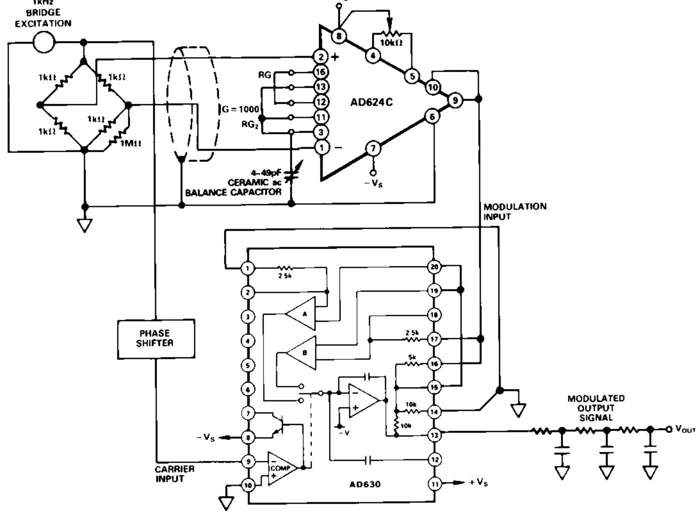


Figure 45. AC Bridge

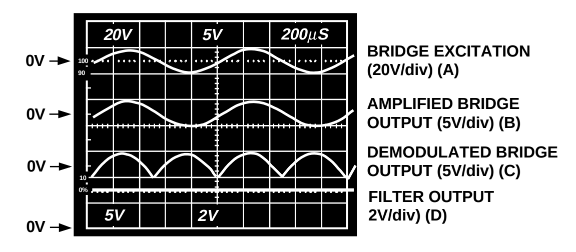


Figure 46. AC Bridge Waveforms

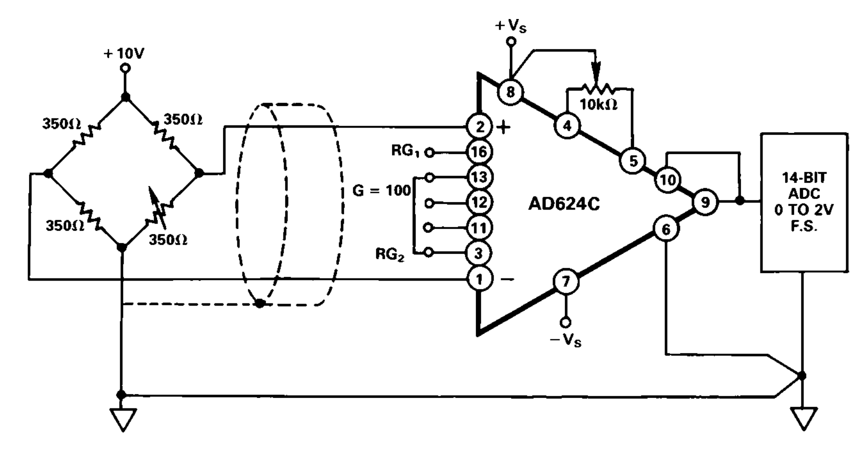


Figure 47. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer. Figure 47 shows a differential transducer, unbalanced by ≈5 Ω, supplying a 0 to 20 mV signal to an AD624C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is –25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to + 85°C (85°C – 25°C = 60°C.)

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (20 ppm = 0.002%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of an auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.002%.

Table II. Error Budget Analysis of AD624CD in Bridge Application

Error Source	AD624C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.1%	±0.1% = 1000 ppm	1000 ppm	1000 ppm	–
Gain Instability	10 ppm	(10 ppm/°C) (60°C) = 600 ppm	–	600 ppm	–
Gain Nonlinearity	±0.001%	±0.001% = 10 ppm	–	–	10 ppm
Input Offset Voltage	±25 µV, RTI	±25 µV/20 mV = ±1250 ppm	1250 ppm	1250 ppm	–
Input Offset Voltage Drift	±0.25 µV/°C	(±0.25 µV/°C) (60°C)= 15 µV 15 µV/20 mV = 750 ppm	–	750 ppm	–
Output Offset Voltage[1]	±2.0 mV	±2.0 mV/20 mV = 1000 ppm	1000 ppm	1000 ppm	–
Output Offset Voltage Drift[1]	±10 µV/°C	(±10 µV/°C) (60°C) = 600 µV 600 µV/20 mV = 300 ppm	–	300 ppm	–
Bias Current–Source Imbalance Error	±15 nA	(±15 nA)(5 Ω) = 0.075 µV 0.075 µV/20mV = 3.75 ppm	3.75 ppm	3.75 ppm	–
Offset Current–Source Imbalance Error	±10 nA	(±10 nA)(5 Ω) = 0.050 µV 0.050 µV/20 mV = 2.5 ppm	2.5 ppm	2.5 ppm	–
Offset Current–Source Resistance Error	±10 nA	(10 nA) (175 Ω) = 1.75 µV 1.75 µV/20 mV = 87.5 ppm	87.5 ppm	87.5 ppm	–
Offset Current–Source Resistance–Drift	±100 pA/°C	(100 pA/°C) (175 Ω) (60°C) = 1 µV 1 µV/20 mV = 50 ppm	–	50 ppm	–
Common-Mode Rejection 5 V dc	115 dB	115 dB = 1.8 ppm × 5 V = 9 µV 9 µV/20 mV = 444 ppm	450 ppm	450 ppm	–
Noise, RTI (0.1 Hz–10 Hz)	0.22 µV p-p	0.22 µV p-p/20 mV = 10 ppm	–	–	10 ppm
		Total Error	3793.75 ppm	5493.75 ppm	20 ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

For a comprehensive study of instrumentation amplifier design and applications, refer to the *Instrumentation Amplifier Application Guide*, available free from Analog Devices.

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